REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

Claims 53-56 stand rejected under 35 U.S.C. §103(a) as allegedly obvious over U.S. Patent No. 5,945,704 to Schrems, et. al. ("Schrems, et al.") in view of U.S. Patent No. 6,174,756 to Gambino, et al. ("Gambino, et al.") and U.S. Patent No. 5,474,946 to Ajit, et al. ("Ajit, et al."). Claims 57-59 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Schrems, et. al. in view of Gambino, et al., and further in view of U.S. Patent No. 5,525,531 to Bronner, et al. ("Bronner, et al.").

Applicants submit that the Examiner has failed to meet his burden to provide a *prima facia* case of obviousness, because the applied references fail to teach or suggest applicants' claimed structure comprising a gate conductor guard ring formed around an array region on top of an isolation region, as recited in Claim 53. "To establish a prima facie case of obviousness of a claimed invention all the claimed limitations must be taught or suggested by the prior art" *In re Wilson,* 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970).

Claim 53 recites a dual workfunction high-performance support MOSFET/EDRAM array comprising at least one support region and at least one array region, said array region and said support region being separated by an isolation region, and *at least a gate conductor guard ring formed around said array region on top of said isolation region*, wherein said gate conductor guard ring prevents trapping of a stringer of gate conductor polysilicon on said isolation region.

Applicants disclose, referring to Page 3, lines 5-11 of the present specification, that the trapping of a stringer of polysilicon in the isolation region can be avoided by positioning a gate conductor guard ring 65 around the array region of a MOSFET/EDRAM structure and *atop an isolation region* 16. Applicants further disclose, referring to Page 3, lines 5-11, that the presence of the gate conductor guard ring 65 provides an internal protection scheme, which prevents the designer from placing a gate conductor across the isolation region 16; therefore reducing the incidence of stringer formation. In order for the gate conductor guard ring 65 to prevent the designer from depositing gate conductor across the isolation region 16; the gate conductor guard ring 65 *must be atop the isolation region* 16, as depicted in FIGS. 9-12.

First, with respect to Claim 53, the Examiner has noted on Page 3 of the instant Office Action, that the principle reference, i.e., Schrems, et al., fails to disclose the following: at least a gate conductor guard ring formed around an array region *on top of said isolation region*, wherein said gate conductor guard ring prevents trapping of a stringer of gate conductor polysilicon on said isolation region. Since Schrems, et al. do not teach or suggest the presence of a guard ring, and the fact that the principle reference does not teach or suggest the presence of a support region, let alone a support region that is separated from the array region by a gate conductor guard ring positioned atop an isolation region, Claims 53-56 are not rendered obvious by Schrems, et al.

Gambino, et al. fail to fulfill the deficiencies of the primary reference, Schrems, et al., since the applied secondary reference also fails to teach or suggest, "at least a *gate conductor guard ring formed around an array region on top of said isolation region*, wherein said gate conductor guard ring prevents trapping of a stringer of gate conductor

polysilicon on said isolation region", as recited in Claim 53. Gambino, et al. disclose a method for forming deep junction implants in one region of the device without affecting the implant of a second region of the integrated circuit. Gambino, et al. disclose an array region 130; a support region 110; and an isolation region 150. Gambino, et al. do not teach or suggest a gate conductor guard ring and therefore fail to teach or suggest forming a gate conductor guard ring atop an isolation region, as recited in Claim 53. As such, Claims 53-56 are not rendered obvious by the combined disclosures of Schrem, et al. and Gambino, et al.

Ajit, et al. also fail to fulfill the deficiencies of the applied references, since this secondary reference also fails to teach or suggest, "at least a gate conductor guard ring 65 formed around an array region 12 *on top of said isolation region* 16, wherein said gate conductor guard ring 65 *prevents trapping of a stringer of gate conductor polysilicon on said isolation region 16*", as recited in Claim 53.

Applicants observe referring to Column 3, line 29-31, that Ajit, et al. make reference to a guard rings being formed from polysilicon strips 20, 21, 24, and 25, where the guard rings are utilized as a mask during a boron implant process. The boron implant is conducted at energy sufficient to produce P-type regions 30, 31, 35, 36 in an n-type epitaxial Si layer 12. Applicants further submit that the Ajit, et al. reference to "guard rings" is only to convey that rings of polysilicon are utilized as hard masks in order to produce doped device regions during a two step masking process which critically aligns the source and drain regions of a MOSFET device. Applicant note that there is no discussion throughout Ajit, et al. of trench isolation regions; the formation of polysilicon stringers atop trench isolation region; or the use of guard ring to reduce the incidence of

polysilicon stringer formation throughout the Ajit, et al. reference. Therefore, Ajit, et al. fails to disclose positioning a guard ring atop an isolation region, as recited in Claim 53.

Applicants further submit that the Ajit, et al. reference teaches away from the claimed invention where a guard ring 65 is positioned atop an isolation region 16 and prevents the formation of polysilicon stringers, as recited in Claim 53. A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore and Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983). Ajit, et al. disclose where the polysilicon rings 20, 21, 24, 25 are used as block masks during device region implantation steps. Therefore, since one of ordinary skill in the art would recognize that there is no need to block an isolation region from device region implants; Ajit, et al. teach away from positioning guard rings atop an isolation region, as recited in Claim 53.

Applicants find no motivation in the combined disclosures of Schrems, et al., Gambino, and Ajit, et al. to modify their disclosed structures to arrive at applicants' claimed structure recited in Claims 53-56. There is no motivation in the applied references that teaches or suggests modifying the structures disclosed therein to include applicants' claimed structure which includes a gate conductor guard ring 65 formed around an array region and *atop an isolation region* 16, as recited in Claim 53. This rejection is thus improper since the prior art *does not* suggest this drastic modification. The law requires that a prior art reference provide some teaching, suggestion, or motivation to make the modification obvious.

In light of the above remarks, applicants respectfully request that the rejection to Claims 53-56 under 35 U.S.C. §103 citing the combined disclosures of Schrems, et al., Gambino and Ajit, et al. be withdrawn.

In regard to the obviousness rejection of Claims 57-59 based on the combination of Schrems, et al., Gambino, et al.; and Bronner, et al., Claim 57 recites "a dual workfunction high-performance support MOSFET/EDRAM array comprising at least one support region having a local interconnect formed therein, and at least one array region having at least one wordline formed therein, said at least one array region and said at least one support region are separated by an isolation region, and at *least one wordline and said local interconnect are comprised of identical material*".

Applicants submit that the applied references do not fulfill the requirements to support a prima facie case of obviousness with respect to Claim 57. "To establish a prima facie case of obviousness of a claimed invention all the claimed limitations must be taught or suggested by the prior art". In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970). Schrems, et al. disclose only an array region of a device. Schrems, et al. do not teach or suggest the limitation of *a support region* as recited in Claim 57. Further, Schrems, et al. do not teach at least one support region having a local interconnect formed therein, *where at least one wordline and said interconnect are comprised of identical material*, as recited in Claim 57.

Gambino, et al. fail to fulfill the deficiencies of the primary reference, Schrems, et al., since the secondary reference also fails to teach or suggest a *support region and a local interconnect formed in the support region.* Gambino, et al. disclose a structure

having a second region (array region) 130 and a first region 110, where the first region comprises a semiconducting device 115.

Applicants, referring to Page 19, lines 20-30, disclose forming a local interconnect 94 in the support region 10 of the device by implanting the substrate through a thin oxide layer 46 to form an interconnect diffusion region 90; removing the thin oxide layer 46; and then depositing gate conducting material 54 directly atop the substrate, where the gate conducting material 54 is in electrical contact with the interconnect diffusion region 90. Gambino, et al. disclose where a gate oxide 160 is deposited atop a substrate followed by the deposition of a gate layer 161, which are then patterned forming a gate stack 115 in the first region 110. The incorporation of the gate oxide 160 into gate stack 115, results in a gate conductor that is not in direct contact with the substrate surface.

Additionally, Gambino, et al., disclose forming source and drain regions 117, 118; further supporting that the gate stack 115 is not an interconnect but a semiconducting device, where the devices conductivity is dependent on the thickness of the gate oxide 160. Since Gambino, et al. fail to teach or suggest an interconnect in the support region of the device, Gambino, et al. also fail to teach or suggest a structure having a wordline and interconnect, where the wordline and interconnect comprise the same material. Therefore, Gambino, et al. do not teach or suggest a support region having an interconnect, where the interconnect and wordline comprise of the same material, as recited in Claim 57.

Bronner et al. also fail to fulfill the deficiencies of the applied references, since this applied secondary reference also fails to teach or suggest a local interconnect formed

in the support region and *where the local interconnect and wordline of the device comprise an identical material*, as recited in Claim 57. It is the Examiner's position in the present Office Action, that "Bronner, et al. discloses wordlines and interconnects made of the same material (For Example: See Column 3 lines 44-67)." Applicants respectfully disagree and present the following.

Applicants disclose, referring to FIG. 24, where a local interconnect 94 comprising the same materials as the opposing wordline, those structures comprising wordline conductor 54, being W/WN. Referring to the passage of Bronner, et al. cited by the Examiner, Column 3, lines 44-67, Bronner, et al. disclose where layers "322, 315 and 310 are etched to define the gate, wordlines (and optionally, local interconnects) both in the array and outside it." Layer 322 represents a cap layer; layer 315 represents a second polysilicon layer and layer 310 represents a first polysilicon layer. Applicants submit that prior to etching layers 322, 315 and 310, Bonner, et al. disclose masking the support region and processing the array region, where during array processing the height of the polysilicon layer 310 is reduced. *See* Bonner, Column 3, lines 44-65. Bonner, et al. further disclose that the original height of the first polysilicon layer 310 in the array region is thereafter restored by depositing a second polysilicon layer 315 until the original height of the first polysilicon layer 310 within the array region is restored; resulting a composite gate structure including layers 310, 315.

Applicants note, referring to Column 4, lines 1-5, that Bonner, et al. further disclose that the second polysilicon layer 315 is deposited in the array region to produce a uniform gate height between the array and support regions. The height of the first polysilicon layer 310 in the support region remains constant and does not include second

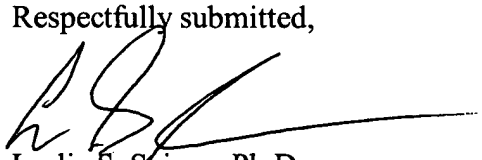
polysilicon layer 315 since the height of the first polysilicon layer is not reduced during array processing due to being protected by the masking. Therefore, the support region comprises gate or interconnect structures consisting only of first polysilicon layer 310. Therefore, since the array region consists of composite structures 310,315 and the support region structures consist solely of layer 310; Bonner, et al. fail to disclose where *at least one wordline and said local interconnect are comprised of identical material.*

Applicants find no motivation in the combined disclosures of Schrems, et. al., Gambino, et al., and Bronner, et al. to modify their disclosed structures to arrive at applicants' claimed structure recited in Claims 57-59. There is no motivation in the applied references, which suggests modifying the structures disclosed therein to include applicants' claimed structure, which includes at least one support region 14 having a local interconnect 94, where are least one wordline 54 and the local interconnect 94 are comprised of identical material as recited in Claim 57. This rejection is thus improper since the prior art does not suggest this drastic modification. The law requires that a prior art reference provide some teaching, suggestion, or motivation to make the modification obvious.

Based on the above remarks the rejection of the Claims 57-59 under 35 U.S.C. §103 has been obviated. Applicants respectfully request reconsideration and withdrawal of the instant rejection.

Wherefore, reconsideration and allowance of the claims of the present application is respectfully requested.

Respectfully submitted,



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